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WAYS FOR PROVIDING A HIGH-SPEED ANALOG-TO-DIGITAL CONVERTER WIT--ETC(U)
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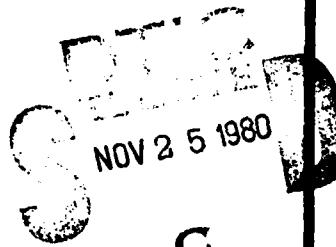
FOREIGN TECHNOLOGY DIVISION



WAYS FOR PROVIDING A HIGH-SPEED ANALOG-TO-DIGITAL
CONVERTER WITH WIDE DYNAMIC RANGE

by

L. A. Dybitskiy, B. I. Shvetskiy, Yu. V. Yuzevich



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By (10) L. A. Dybitskiy, B. I. Shvetskiy
(10) Yu. V. Yuzevich

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U. S. BOARD ON GEOGRAPHIC NAMES TRANSLITERATION SYSTEM

Block	Italic	Transliteration	Block	Italic	Transliteration
А а	А е	А, a	Р р	Р р	Р, r
Б б	Б ъ	В, b	С с	С ѿ	С, s
В в	В ѿ	В, v	Т т	Т ѿ	Т, т
Г г	Г ѿ	Г, g	Ү ү	Ү ү	Ү, ү
Д д	Д Ѹ	Д, d	Ф ф	Ф ф	Ф, f
Е е	Е ѿ	Ye, ye; Е, е*	Х х	Х ѿ	Хх, kh
Ж ж	Ж ѿ	Zh, zh	Ц ц	Ц ѿ	Ts, ts
З з	З ѿ	Z, z	Ч ч	Ч ѿ	Ch, ch
И и	И ѿ	I, i	Ш ш	Ш ѿ	Sh, sh
Й й	Й ѿ	Y, y	Щ ѿ	Щ ѿ	Shch, sch
К к	К ѿ	K, k	Ь ѿ	Ь ѿ	"
Л л	Л ѿ	L, l	Ү ѿ	Ү ѿ	Ү, ү
М м	М ѿ	M, m	Ծ ѿ	Ծ ѿ	"
Н н	Н ѿ	N, n	Э э	Э ѿ	Е, e
О о	О ѿ	O, o	Ӯ ѿ	Ӯ ѿ	Yu, yu
П п	П ѿ	P, p	Я я	Я ѿ	Ya, ya

*ye initially, after vowels, and after ѿ, ѿ; e elsewhere.
When written as є in Russian, transliterate as ѿ or є.

RUSSIAN AND ENGLISH TRIGONOMETRIC FUNCTIONS

Russian	English	Russian	English	Russian	English
sin	sin	sh	sinh	arc sh	sinh
cos	cos	ch	cosh	arc ch	cosh
tg	tan	th	tanh	arc th	tanh
ctg	cot	cth	coth	arc cth	coth
sec	sec	sch	sech	arc sch	sech
cosec	csc	csch	csch	arc csch	csch

Russian English

rot	curl
lg	log

WAYS FOR PROVIDING A HIGH-SPEED ANALOG-TO-DIGITAL CONVERTER WITH WIDE DYNAMIC RANGE

L. A. Dybitskiy, B. I. Shvetskiy, Yu. V. Yuzevich

The problem of providing a large dynamic range in conjunction with a high operating speed and the necessity to process signals of sufficiently high frequency in an ATsP [analog-to-digital converter] is becoming extremely urgent.

Questions of realizing an ATsP which provides the conversion of signals in a band of frequencies from 0 to 100 kHz which corresponds to a rate of change of up to 10^7 V/s within the dynamic range of 80 dB (1 mV-10 V in both polarities) with a five-microsecond conversion time and an error of about 1% are examined below. It is advisable to accomplish the device's realization in accordance with the block-diagram presented in Fig. 1.

The device consists of two parts: an input unit and an encoding converter. The input unit contains a number of scaling amplifiers (1). The encoding converter includes the comparison circuits (2), a logical channel-selection device (3), a commutator for analog signals (4), a high-speed time-pulse ATsP with a narrow dynamic range (5), and a timer which determines the interaction order of the units.

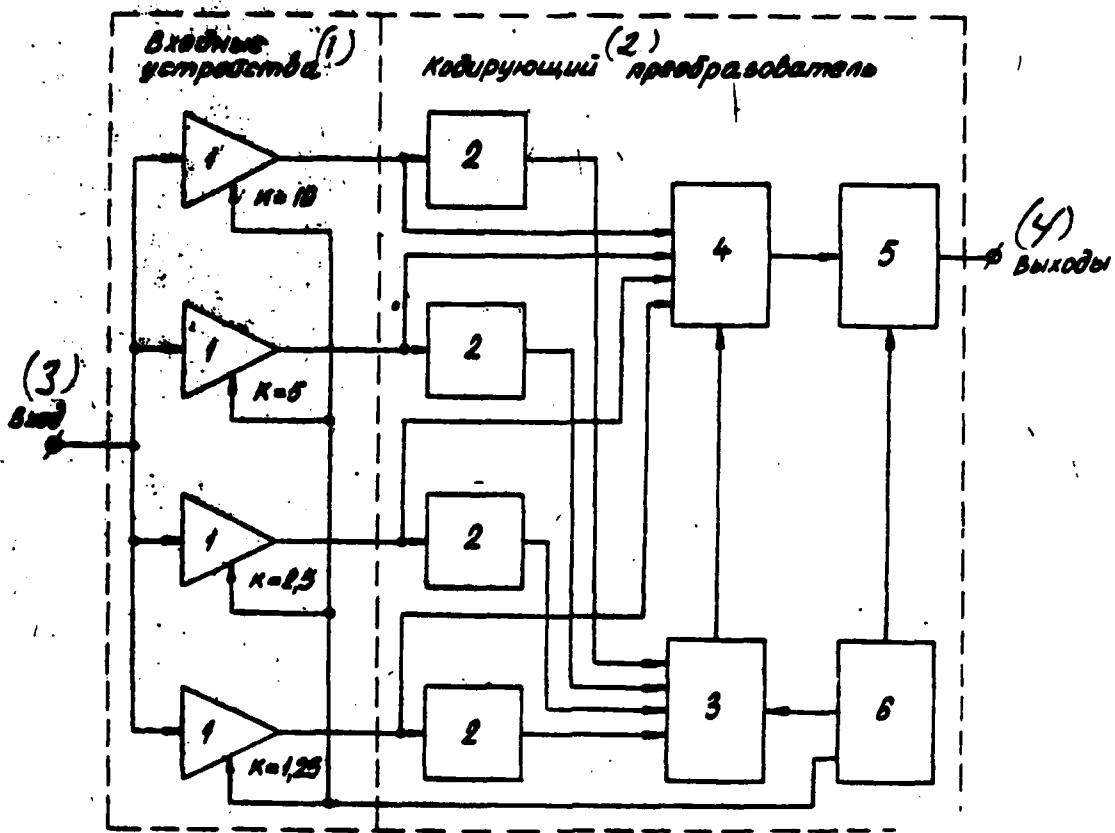


Fig. 1.

KEY: (1) Input unit; (2) Encoding converter; (3) Input; (4) Output.

The scaling amplifiers are controlled by pulses which enter from the timer. The amplification factors of these amplifiers are interconnected by the corresponding scale factors. The storage of the voltage's instantaneous values for the time necessary to convert analog quantities into digital is conducted upon completion of the pulse which arrives from the timer. The voltage arrives at the comparison circuits and the commutator from the amplifiers' outputs. Signals from the comparison circuits control the channel-selection device's operation and determine the signal's arrival from the channel-selection device to the corresponding commutator key according to the pulse from the timer. While being closed the key connects that one of the amplifiers' outputs in which the voltage is the greatest and is within the limits of the ATsP's dynamic range to the input of the time-pulse ATsP. The ATsP accomplishes the conversion

of voltage into a code and a multiplication of the results by a weighting factor which conforms to the selected output-channel.

The selection of the structure and scheme of the units is conducted on the basis of the following considerations.

The scaling amplifier. Its preamplification is necessary in order to convert the input signal at the minimum level of 1 mV. A realization of high-precision amplifiers for the signal with the parameters listed above in contemporary elements requires redundancy in equipment and is solved in the device by the network of amplifiers whose amplification factors are connected by the corresponding scale (Fig. 1).

The task of picking up a signal to the converter is complex. In order to eliminate a dynamic error during quantization a special pick-up scheme - the voltage clamp is used in the device: pre-amplification - a key with a capacitor store - output amplifier - feedback (Fig. 2). This scheme allows the influence of time of pick-up on the precision of the conversion to be eliminated, and a large dynamic range of read voltages to be provided when the pick-up precision is high and the drift of voltage at the output is small as well as to achieve high load characteristic.

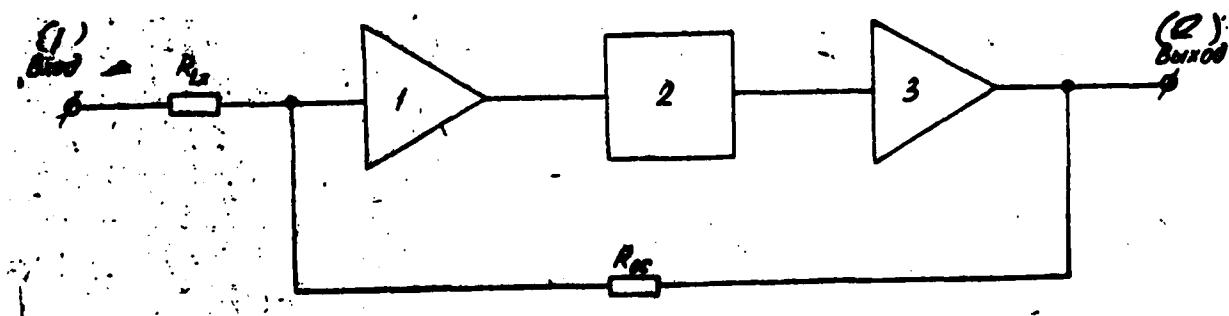


Fig. 2.

KEY: (1) Input; (2) Output.

When the switch is closed the circuit is an operating amplifier. That characteristic allows the functions of scalable amplifiers and clamps in some units to be combined in the instrument the equipment to be substantially reduced, and the precision of the unit to be increased.

The pulse-time converter. The selection of the structure of the converter is determined first of all by the little time allotted to conversion and equals three μ s. In the course of the first 0.5 μ s a set-up of the corresponding output - channel is completed by a method of direct comparison (units 2 in Fig. 1). For the remaining 2.5 μ s the voltage is converted into code by the pulse-time method. The pulse-time method in this case may be considered most optimum. A representation of data at the output of the coding converter is accomplished in a 4-digit binary-decimal code. Such a representation substantially hampers the construction of a high-frequency counter because it requires the use of feedback which reduced the speed of operation [1]. A special structure which provides the counting pulses following with a high frequency and the representation of their number in a binary-decimal code [2] is used in this device. The counter here is purely binary.

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